Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **COMP**
2. **NC**
3. **VFB**
4. **NC**
5. **ISENSE**
6. **NC**
7. **RT/CT**
8. **PWR GND**
9. **GND**
10. **OUTPUT**
11. **VC**
12. **VCC**
13. **NC**
14. **VREF**

**14**

**12**

**11**

**10**

**9**

**1**

**3**

**5**

**7**

**8**

**1844**

**MASK**

**REF**

**NC = No Connection**

**For 8 pin applications:**

**Pads 8&9 are commoned**

**Pads 11&12 are commoned**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: GND**

**Mask Ref: 1844**

**APPROVED BY: DK DIE SIZE .071” X .096” DATE: 4/27/23**

**MFG: TI / UNITRODE THICKNESS .015” P/N: UC1844**

**DG 10.1.2**

#### Rev B, 7/1